

Integrated Antenna With Direct Conversion Circuitry for Broad-Band Millimeter-Wave Communications

Ji-Yong Park, *Student Member, IEEE*, Seong-Sik Jeon, *Student Member, IEEE*, Yuanxun Wang, *Member, IEEE*, and Tatsuo Itoh, *Fellow, IEEE*

Abstract—A compact integrated antenna with direct quadrature conversion circuitry for broad-band millimeter-wave communications is proposed. The conversion circuits include two even-harmonic mixers based on antiparallel diode pairs (APDPs). The equivalent circuit of the APDP derived here provides good agreement with the measured data from 17 to 23 GHz. Overall phase and amplitude imbalance between the in-phase/quadrature (I/Q) output channels are less than 1.2° and 1 dB at IFs of 10 and 100 MHz, respectively. An overall RF power conversion loss of 14.6 dB at the quadrature I/Q channels including the antenna is achieved in the frequency range from 39.75 to 40.25 GHz with a local oscillator (LO) power level of 11.8 dBm. LO leakages at 20 and 40 GHz are -31.5 and -44.8 dBm, respectively. In order to demonstrate the system capabilities for broad-band digital communication, a communication link is built with a pair of the proposed front-ends. Data transmission up to 1-Gb/s data rate for quadrature phase-shift keying modulation is demonstrated.

Index Terms—Antiparallel diode pair (APDP), broad-band millimeter-wave circuit, direct quadrature conversion, integrated patch antenna.

I. INTRODUCTION

CURRENTLY, many communication services requiring high data rate are moving toward millimeter-wave frequencies for larger spectrum availability and more broad-band capability. Thus, low-cost and high-performance millimeter-wave circuits have become desirable for such applications. Compared to the circuits at the lower end of the microwave spectrum, millimeter-wave circuits have the advantages of compact size and light weight. However, there are also many challenges for the design of these millimeter-wave circuits. First, when the frequency is higher, there is usually less power available, which necessitates a low-loss and high power-efficiency design. Second, due to the shorter wavelength at this frequency range, the circuit is more susceptible to design and fabrication errors, which requires careful computer-aided design (CAD) based on accurate device models.

To address these two issues in this context, a millimeter-wave transceiver front-end circuit and the associated CAD methodology are presented. The circuit is based on the integration of a planar antenna and direct quadrature conversion circuit. The direct conversion circuitry has been widely used for digital

millimeter-wave applications. Ashtiani *et al.* introduced direct carrier modulation for 38- and 60-GHz vector modulators and demonstrated quadrature amplitude modulation (QAM) digital communications [1]. Tatu *et al.* built a 23–31-GHz direct-conversion six-port receiver for quadrature phase-shift keying (QPSK) communications [2]. A millimeter-wave mixer integrated with a planar antenna has also been introduced by the authors' group [3], [4]. However, the quadrature channel function, which benefits most of the spectrum efficient communication schemes, has not been supported in the circuits proposed in [3] and [4]. Recently, a direct conversion sub-harmonic in-phase/quadrature (I/Q) mixer has been suggested in authors' group in order to achieve broad-band digital baseband modulation and demodulation [5]. Shimozawa *et al.* proposed a direct conversion receiver using an even-harmonic mixer (EHM) with an antiparallel diode pair (APDP) [6]. The main reason for this is that a subharmonic local oscillator (LO) can be used in place of an expensive millimeter-wave LO and its balanced structure suppresses the first-order mixing products. Therefore, it provides good performance in terms of conversion loss, as well as AM noise suppression from the LO [7]–[9]. Cohn *et al.* and Schneider *et al.* analyzed the harmonic mixing with APDP and demonstrated it has only even-harmonic mixing products in the form of symmetric conduction periods [7], [10]. The EHMs with APDP have been proposed for many applications such as modulators [11], [12], millimeter-wave image-rejection mixers [13], direct conversion mixers [14], [15] as well as millimeter-wave mixers [16], [17].

In this paper, using EHMs based on a pair of APDPs, the direct conversion circuitry is realized to provide both I/Q phase channels. The direct conversion circuitry is integrated with a 40-GHz planar patch antenna with impedance matched to $50\ \Omega$. With two such front-ends, a communication link including a transmitter and receiver is built. The proposed approach has a threefold advantage. First, directly integrating the antenna with the front-end RF circuits realizes a compact millimeter-wave front-end and reduces the interconnection loss between the antenna and circuits, which is an important issue at millimeter-wave frequencies [18]. Secondly, the circuit provides the direct conversion capability for digitally modulated signals, which eliminates the need of items such as an IF mixer, image rejection filters, and saves printed circuit board space [9], [19]–[21]. More importantly, the existence of I/Q channels for direct conversion is suited for various frequency- and phase-modulation systems such as binary phase-shift keying (BPSK), QPSK, QAM, frequency-shift keying (FSK), etc. Furthermore, I/Q channels can naturally

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The authors are with the Electrical Engineering Department and Microwave Electronics Laboratory, University of California at Los Angeles, Los Angeles, CA 90095 USA (e-mail: jypark@ee.ucla.edu).

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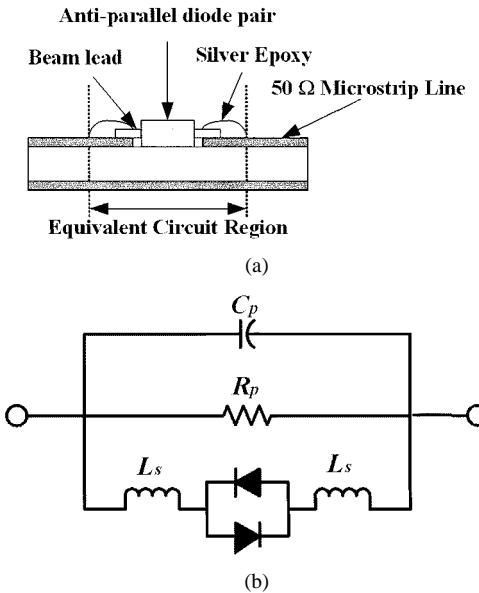


Fig. 1. (a) Profile and (b) equivalent circuit of an APDP mounted on a $50\text{-}\Omega$ microstrip line.

provide broad-band phase control in an adaptive beamforming array system with a hybrid beamformer [22], [23]. Lastly, due to the high carrier frequency of the millimeter-wave front-ends, broad-band digital communication over gigabits per second can be easily achieved with applications in short-range indoor wireless communications of high-speed digital video signals.

This paper is organized as follows. The equivalent circuit of an APDP is first given for CAD purposes. The designed layout of the front-end is then shown. The performance of the quadrature mixer circuit is validated with measured results. Finally, a communication link is set up by using a pair of the proposed front-ends to examine the data modulation, transmitting, receiving, and demodulation capabilities. The link test shows successful transmission of QPSK data up to 1-Gb/s data rate.

II. CIRCUIT CAD AND LAYOUT

A. APDP

The profile and equivalent circuit of a GaAs beam lead Schottky barrier APDP (Agilent HSCH-9251) mounted on a $50\text{-}\Omega$ microstrip line are depicted in Fig. 1. This model includes the leads of the APDP, silver epoxy, and a $50\text{-}\Omega$ microstrip line at both terminals in order to take into account the microstrip-to-chip transition shown in Fig. 1(a). The leads and contacts of the diode create a shunt capacitance C_p and a series inductance L_s [24], where C_p includes the capacitance values between diode leads and the strip ground plane, as well as between both leads through the dielectric substrate and air. The loss of mutual coupling between two leads of the APDP is modeled by a shunt resistance R_p . The measured S -parameters are used to curve-fit appropriate values for C_p , L_s , and R_p in the diode equivalent circuit. Each C_p , L_s , and R_p value is optimized, while intrinsic diode parameters are provided by Agilent's data sheet.

In order to obtain the values of parameters in Fig. 1(b), the APDP mounted on a $50\text{-}\Omega$ microstrip line is terminated. Fig. 2

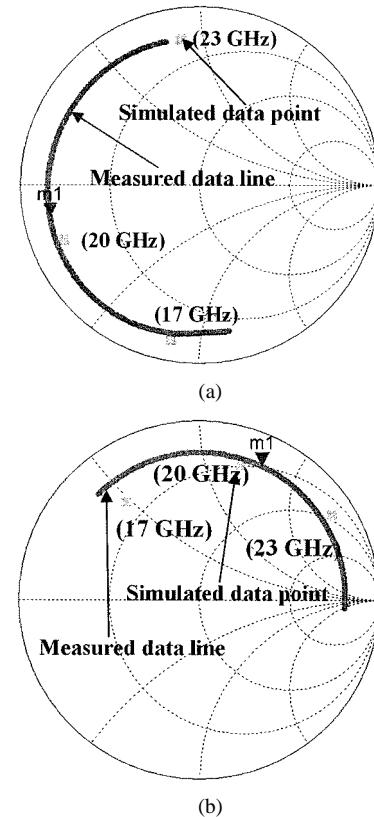


Fig. 2. Measured and simulated S_{11} -parameter data lines and points of an APDP mounted on a $50\text{-}\Omega$ microstrip line. (a) Bias: 0 V. (b) Bias: 0.8 V.

shows the measured diode S_{11} -parameters of the diode from 17 to 23 GHz along with simulated S_{11} -parameter points at 17, 20, and 23 GHz, respectively. The bias point of 0.8 V in the APDP provides the highest forward current before saturation at room temperature (25°C). Measured and simulated S_{11} -parameters are compared at the bias point, as shown in Fig. 2(b). Each "m1" point on the measured S_{11} -parameter data line in Fig. 2(a) and (b) corresponds to an LO pump of 20 GHz for the EHM. The measured results agree well with the simulated data points from 17 to 23 GHz.

B. Integrated Patch Antenna With Direct Quadrature Conversion Circuitry

In order to achieve good phase and amplitude balance of an even-harmonic direct quadrature mixer, a 20-GHz Wilkinson power divider with a 45° phase delay line, as illustrated in Fig. 3(a), is simulated. The 45° phase delay line is connected to one of Wilkinson power divider arms for the Q channel mixer. Figs. 3(b) and (c) shows good power amplitude balance between S_{21} and S_{31} , as well as good matching and isolation from S_{11} and S_{32} , respectively. Fig. 3(d) shows good 45° phase balance at 20 GHz. After mixing an RF of 40 GHz with an LO of 20 GHz in the diodes, the phase delay line of 45° from one of paths in the 20-GHz Wilkinson power divider makes I and Q channels.

The EHM is designed with the help of the equivalent circuit of Fig. 1(b). Open and short stubs are perpendicularly connected at each port of the equivalent circuit of the APDP [25]. Both stubs are a quarter-wave length at LO of 20 GHz and a half-wave

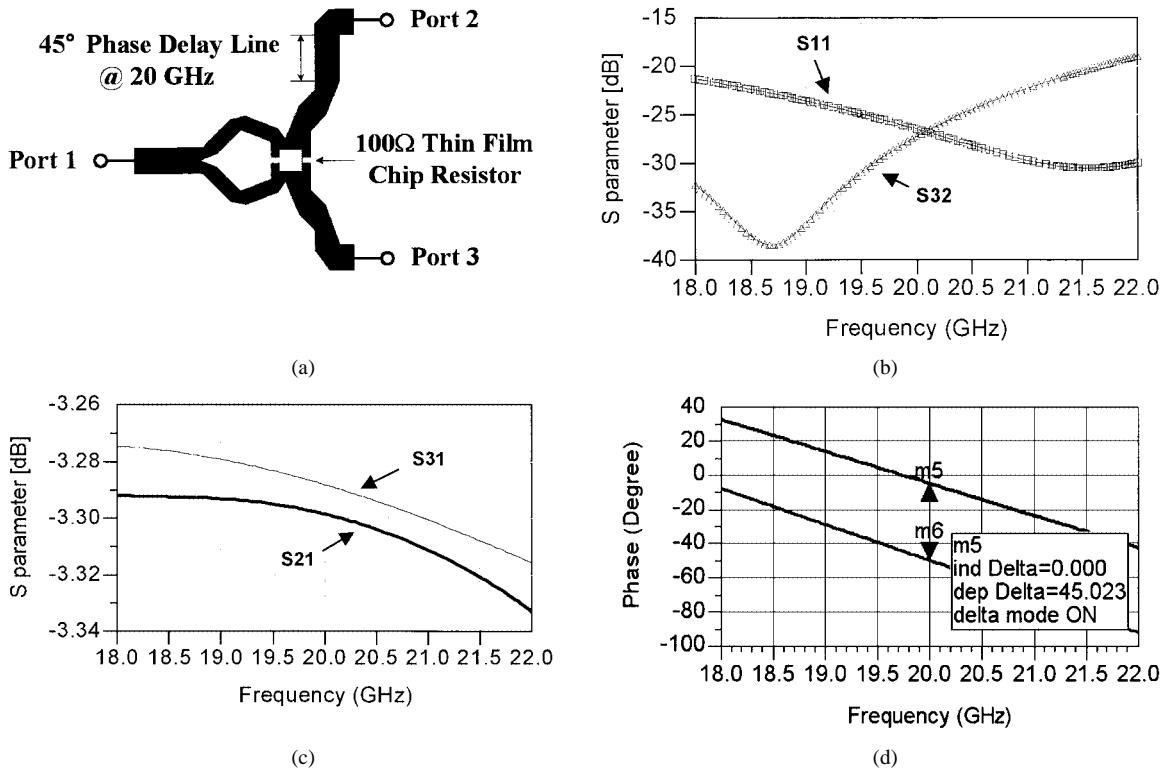


Fig. 3. Circuit layout and simulated results of 20-GHz Wilkinson power divider with a 50- Ω phase delay line of 45°. (a) Circuit layout. (b) S_{11} and S_{32} versus frequency. (c) S_{21} and S_{31} versus frequency. (d) Phases versus frequency for S_{21} and S_{31} .

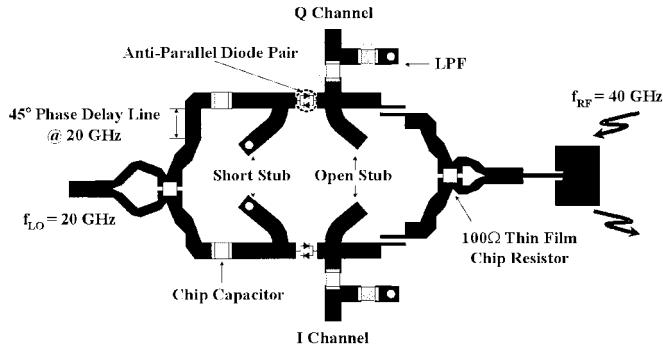


Fig. 4. Circuit architecture of the integrated antenna with direct conversion circuitry (circuit size: 2.54×1.85 cm 2).

length at RF of 40 GHz. When the RF and LO are applied to each port with an open stub and a port with a short stub, the impedances of open and short stubs are infinite for each RF and LO. However, RF and LO leakages are terminated at each short and open stub after the RF and LO pass through the APDP. Therefore, the mixer features low conversion loss with the above circuit. The other passive components, namely, a microstrip patch antenna, Wilkinson power divider, and bandpass filter (BPF) at 40 GHz are designed and integrated with two identical EHMs and the described 20-GHz Wilkinson power divider with a phase delay line of 45°. Fig. 4 shows the whole circuit architecture of the proposed direct conversion circuitry consisting of the APDP EHMs integrated with the microstrip patch antenna at a 40-GHz RF carrier.

BPFs are designed for LO and baseband decoupling. Therefore, LO leakage from the antenna of the transmitter can be reduced. The proposed circuits are fabricated on an RT/Duroid

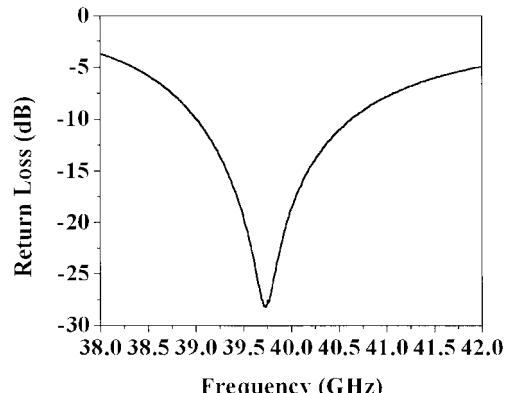


Fig. 5. Measured return loss of the microstrip patch antenna.

5880 with a dielectric constant of 2.2 and a substrate thickness of 0.254 mm. Agilent's ADS circuit and Momentum full-wave simulator is used to predict the mixer performance and all relevant antenna and other passive circuits' characteristics. In order to establish a communication link, two identical integrated front-ends are fabricated. One acts as a modulator and the other acts as a demodulator.

III. MEASUREMENT AND DISCUSSION

A. RF Characteristics of an Integrated Antenna With Direct Conversion Circuitry

Fig. 5 shows the return loss of the microstrip patch antenna. The patch size, not including the quarter-wave transformer, is 2.24×3.05 mm 2 . The resonant frequency of the antenna is 39.73 GHz, and its -10 -dB bandwidth is 1.62 GHz, i.e., 4.1%.

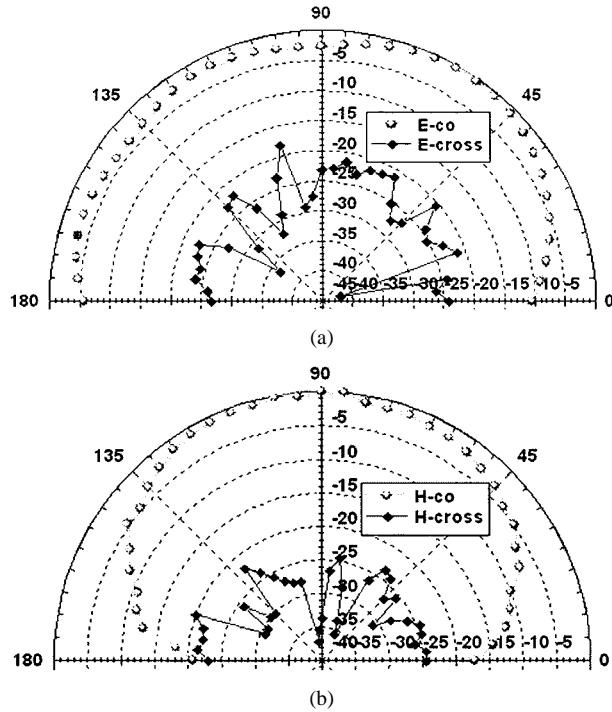
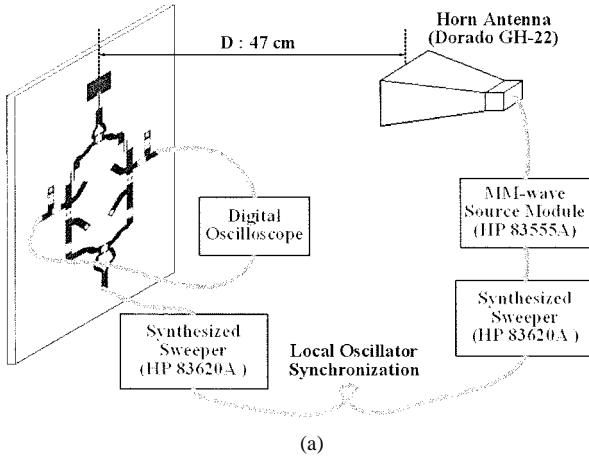
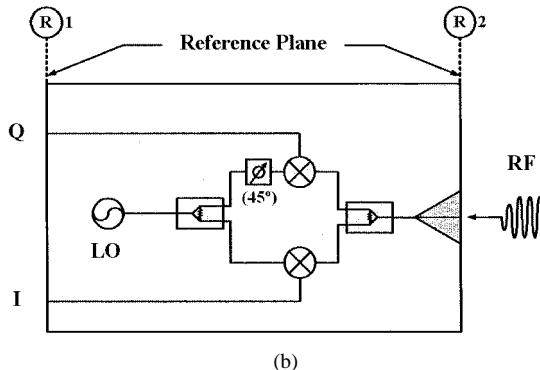


Fig. 6. Co- and cross-polarized radiation patterns of the microstrip patch antenna at 40 GHz. (a) E -plane (b) H -plane.



(a)



(b)

Fig. 7. RF characteristic experimental test setup and block diagram for calculating conversion loss of the described integrated antenna with direct conversion circuitry.

Fig. 6 shows the measured co- and cross-polarized radiation patterns in the E - and H -plane of the microstrip patch antenna at 40 GHz. The cross-polarization levels are lower than -19 dB

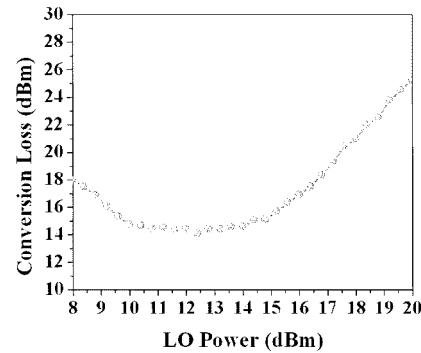


Fig. 8. Measured conversion loss as a function of LO power at IF frequency = 100 MHz (RF power is defined as the power intercepted by the antenna).

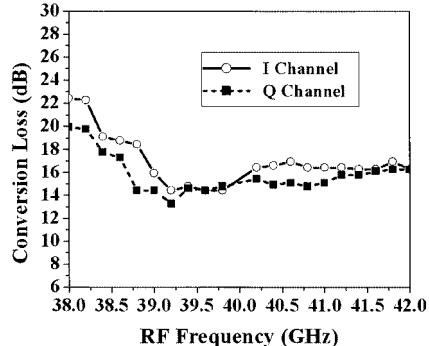


Fig. 9. Conversion loss as a function of RF frequency for I and Q channels at LO power = 11.8 dBm (RF power is defined as the power intercepted by the antenna).

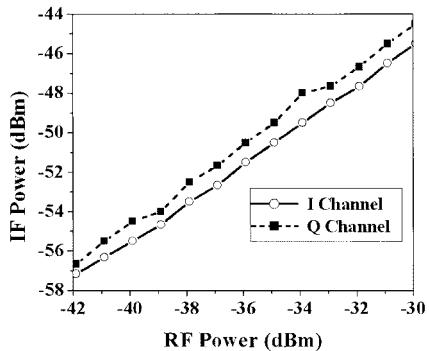


Fig. 10. Measured IF power as a function of RF power for I and Q channels at IF frequency = 100 MHz with LO power = 11.8 dBm.

for the E -plane and -20 dB for the H -plane, respectively, from 45° to 135° . The BPF with return loss of 15 dB is achieved at the center frequency of 40 GHz with 400-MHz bandwidth.

In order to measure the RF characteristics of the described integrated antenna with the direct conversion circuitry, a transmitter including an HP 83620A synthesized sweeper, an HP 83555A millimeter-wave source module, and a Dorado GH-22 horn antenna is set up at the distance of 47 cm for far-field pattern measurement. The circuit is connected to a digital oscilloscope, as shown in Fig. 7(a). The two synthesized sweepers for LOs of the transmitter and receiver are synchronized using a time base signal in both synthesized sweepers. The RF power is defined as the power intercepted by the antenna at reference plane $\textcircled{R}2$, as shown in Fig. 7(b). This indirect calibration method is free of measurement errors due to cable losses and other devices in millimeter wavelengths [26]. Fig. 8

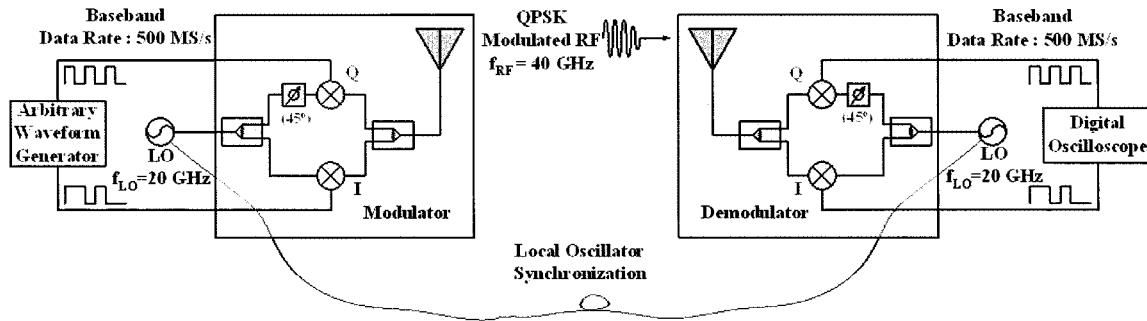


Fig. 11. Block diagram of the modulation/demodulation including two proposed circuits.

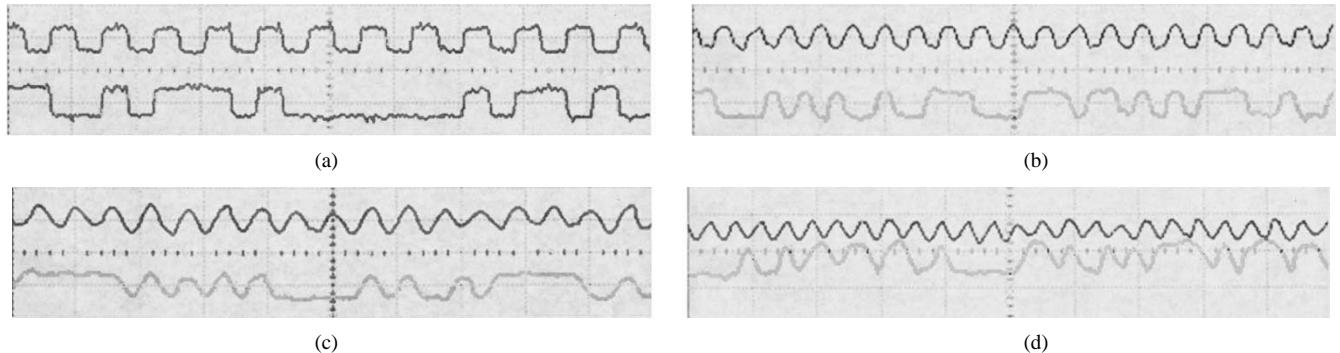


Fig. 12. Demodulated 0101 binary sequences and pseudorandom bit sequences at I and Q channels of the integrated antenna with direct conversion circuitry (a) 50 Ms/s (50 ns/div, 2 mV/div). (b) 200 Ms/s (20 ns/div, 2 mV/div). (c) 350 Ms/s (10 ns/div, 2 mV/div). (d) 500 Ms/s (20 ns/div, 2 mV/div).

shows the average conversion loss for I and Q channels as a function of LO power for an IF of 100 MHz, where conversion loss is defined by the ratio of the RF power at $\textcircled{R}2$ to the IF power at $\textcircled{R}1$, as shown in Fig. 7(b). The available RF power is calculated by using the Friis' transmission formula. The conversion loss is better than 15 dB from 10 to 14 dBm of LO power. As compared to a simulated conversion loss of 12 dB with an LO power of 10 dBm, the measured conversion loss is 2 dB higher with 2 dBm higher LO power because of the higher loss of duroid substrate in millimeter-wave bands. 1.2° phase deviation is measured between the I and Q channels from ideal quadrature phase at an IF of 10 MHz.

Fig. 9 shows the measured conversion loss as a function of the RF carriers with an LO power of 11.8 dBm. Flat power balance between I and Q channels is observed. Within the frequency range from 39.75 to 40.25 GHz (500 MHz) imbalance between I and Q channels is lower than 1 dB and the average conversion loss is 14.6 dB for both channels. The integrated antenna with direct conversion circuitry features good I and Q phase and power balance, which ensures low crosstalk between the two baseband channels [20]. Fig. 10 shows the measured IF power as a function of RF power for the I and Q channels at an IF of 100 MHz for LO power of 11.8 dBm. Both the I and Q channel outputs show good power linearity as the RF power is increased. LO leakages are -31.5 dBm and -44.8 dBm at 20 and 40 GHz, respectively.

B. Communication Link Test for QPSK Signal

The communication link test setup is depicted in Fig. 11. A pair of the proposed front-ends is used as a modulator/transmitter and a demodulator/receiver system. The link budget for

RX/TX is as follows: a patch antenna gain of 3 dBi/40 GHz, a Wilkinson power divider of -3.5 dB/40 GHz, a BPF of -1 dB/40 GHz (the bandwidth of 15-dB return loss: 400 MHz), RX/TX EHM of -14 dB/40 GHz, a low-pass filter (LPF) of -3 dB/1-GHz cutoff frequency, and free-space loss of -29 dB. The data is modulated in QPSK format and the modulation/demodulation is straightforward in the proposed system. A SONY Tektronix AWG520 arbitrary waveform generator is used to generate the baseband data at a sampling rate up to 1 GS/s. Unfiltered 0101 binary sequences and pseudorandom bit sequences are applied to the modulator at each I and Q channel of the circuitry. Two sequential demodulated baseband waveforms for both I and Q channels are shown in Fig. 12 after modulation, transmission, reception, and demodulation.

Four different baud rates are set at 50, 200, 350, and 500 Ms/s, corresponding to data rates of 100, 400, 700, and 1 Gb/s, respectively, with QPSK modulation. From Fig. 12, the communication link demonstrates the potential of digital transmission up to 1 Gb/s. As the bandwidth is increased, more distortion of the pulse shape is observed. This is mainly due to the limited sampling rate of the arbitrary waveform generator (1 GS/s), which does not support frequency components of the digital pulses above 500 MHz. The other error sources contributing to the signal distortions include the dispersion of the signal channel such as antenna bandwidth limitation, and the nonideal band-limiting effects of the LPFs and BPFs. For digital modulation, the raised cosine filter can be applied to reduce the cross-symbol interference. Fig. 13 shows eye diagrams to provide a visual representation of the performance of the communication link transmitting data in QPSK format. It is obtained by sending the 0101 binary sequences and pseudorandom

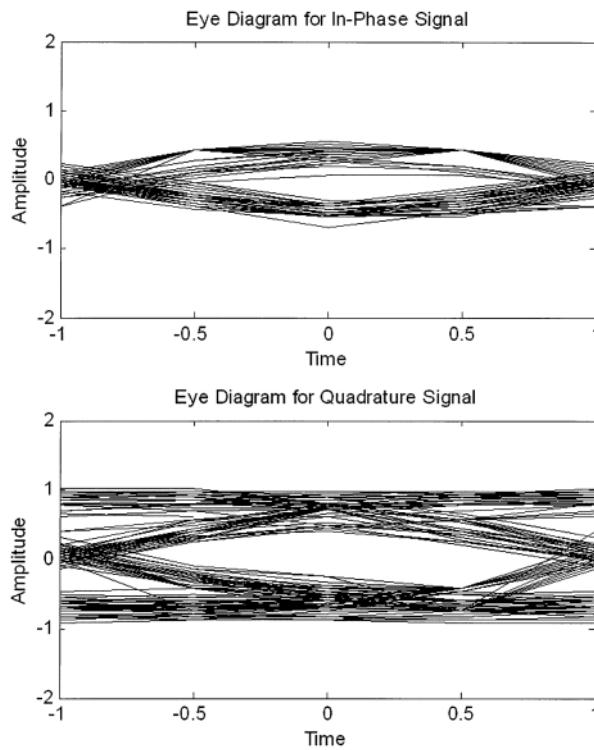


Fig. 13. Eye diagrams of the demodulated 0101 binary sequences and pseudorandom bit sequences at I and Q channels for 500 Ms/s (1 Gb/s).

bit sequences over I and Q channels. The demodulated data are exported from a digital oscilloscope and plotted over time using MATLAB. Due to the signal attenuation and noise, the eye diagram exhibits some narrowing. A power amplifier at the transmitter and a low-noise amplifier at the receiver can be implemented in order to improve communication performance in terms of noise figure and gain.

The broad-band communication capability of the proposed circuit is potentially promising for many advanced wireless applications. For instance, this configuration can be extended to unlicensed 60-GHz short-range indoor wireless communication systems. One of the interesting features of the proposed front-end is that it fits well into the broad adaptive beamforming array system currently under study in the authors' group [22], [23].

IV. CONCLUSION

Millimeter-wave direct quadrature conversion circuitry has been directly integrated with a 40-GHz microstrip patch antenna. The integration and direct conversion system enable a simple, compact, light-weight, and low-cost design of transceiver systems at millimeter-wave frequency. Furthermore, the digital data transmission at 1-Gb/s data rate in QPSK format has been demonstrated. It is expected that the proposed front-end circuits will find extensive applications in broad-band wireless communications.

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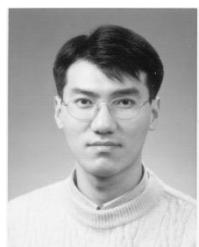
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Ji-Yong Park (S'98) was born in Seoul, Korea, in 1970. He received the B.S. and M.S. degrees in radio science and engineering from Kwangwoon University (KU), Seoul, Korea in 1997 and 1999, respectively, and is currently working toward the Ph.D. degree in electrical engineering at the University of California at Los Angeles (UCLA).

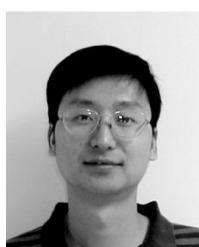
From 1999 to 2000, he was an Intern Researcher in radio science and engineering at KU, during which time he was sponsored by the Korea Science and Engineering Foundation. As a Graduate Student Research Assistant with UCLA, his research interests include microwave and millimeter-wave receivers and phased arrays for wireless communications, integrated circuits, and antennas.



Seong-Sik Jeon (S'99) was born in Seoul, Korea, in 1968. He received the B.S. and M.S. degrees in electronic engineering from Yonsei University, Seoul, Korea, in 1991, 1993 respectively, and is currently working toward the Ph.D. degree in electrical engineering at the University of California at Los Angeles (UCLA).

From 1993 to 1998, he was a Research Engineer with LG Electronics, Seoul, Korea. His research interests include phased-array antennas, millimeter-wave RF front ends, and mobile communication systems.

Mr. Jeon was a recipient of the Honorable Mention Award in the Student Paper Competition at the 2001 IEEE Microwave Theory and Techniques Society (IEEE MTT-S) International Microwave Symposium (IMS).



Yuanxun Wang (S'96–M'99) received the B.S. degree in electrical engineering from the University of Science and Technology of China (USTC), Hefei, China, in 1993, and the M.S. and Ph.D. degrees in electrical engineering from the University of Texas at Austin, in 1996 and 1999, respectively.

From 1995 to 1999, he was a Research Assistant with the Department of Electrical and Computer Engineering, University of Texas at Austin. From 1999 to 2002, he was a Research Engineer and Lecturer with the Department of Electrical Engineering, University of California at Los Angeles (UCLA), prior to joining the faculty. Since 2002, he has been an Assistant Professor with the Electrical Engineering Department, UCLA. He has authored and coauthored over 60 refereed journal and conference papers. His research has focused on high-performance antenna array and microwave amplifier systems for wireless communication and radar, as well as numerical modeling techniques. His current research interests feature the fusion of signal processing and circuit techniques in microwave system design.

Dr. Wang is a member of The International Society for Optical Engineers (SPIE).



Tatsuo Itoh (S'69–M'69–SM'74–F'82) received the Ph.D. degree in electrical engineering from the University of Illinois at Urbana-Champaign, in 1969.

From September 1966 to April 1976, he was with the Electrical Engineering Department, University of Illinois at Urbana-Champaign. From April 1976 to August 1977, he was a Senior Research Engineer with the Radio Physics Laboratory, SRI International, Menlo Park, CA. From August 1977 to June 1978, he was an Associate Professor at the University of Kentucky, Lexington. In July 1978,

he joined the faculty at The University of Texas at Austin, where he became a Professor of electrical engineering in 1981 and Director of the Electrical Engineering Research Laboratory in 1984. During the summer of 1979, he was a Guest Researcher at AEG-Telefunken, Ulm, Germany. In September 1983, he was selected to hold the Hayden Head Centennial Professorship of Engineering at The University of Texas at Austin. In September 1984, he was appointed Associate Chairman for Research and Planning of the Electrical and Computer Engineering Department, The University of Texas at Austin. In January 1991, he joined the University of California at Los Angeles (UCLA), as Professor of electrical engineering and Holder of the TRW Endowed Chair in Microwave and Millimeter Wave Electronics. He was an Honorary Visiting Professor at the Nanjing Institute of Technology, Nanjing, China, and at the Japan Defense Academy. In April 1994, he became an Adjunct Research Officer for the Communications Research Laboratory, Ministry of Post and Telecommunication, Japan. He currently holds a Visiting Professorship at The University of Leeds, Leeds, U.K., and is an External Examiner of the Graduate Program of the City University of Hong Kong. He has authored or coauthored 274 journal publications, 540 refereed conference presentations, and 30 books/book chapters in the area of microwaves, millimeter-waves, antennas and numerical electromagnetics. He has generated 49 Ph.D. students.

Dr. Itoh is a member of the Institute of Electronics and Communication Engineers of Japan and Commissions B and D of USNC/URSI. He became an Honorary Life Member of the IEEE Microwave Theory and Techniques Society (IEEE MTT-S) in 1994. He was the editor-in-chief of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES (1983–1985) and the IEEE MICROWAVE AND GUIDED WAVE LETTERS (1991–1994). He serves on the Administrative Committee of the IEEE MTT-S. He was vice president of the IEEE MTT-S in 1989 and president in 1990. He was the chairman of USNC/URSI Commission D (1988–1990), and Chairman of Commission D of the International URSI (1993–1996). He is the chair of the Long Range Planning Committee of URSI. He serves on advisory boards and committees of a number of organizations. He has been the recipient of a number of awards, including the 1998 Shida Award presented by the Japanese Ministry of Post and Telecommunications, the 1998 Japan Microwave Prize, the 2000 IEEE Third Millennium Medal, and the 2000 IEEE MTT-S Distinguished Educator Award.